In the Claims:

Claims 1-11 (Cancelled)

12. (Previously Presented) A method of producing a mask-making member, said member has a plurality of pattern formation regions in which mask circuit patterns are to be formed, and a supporting region in which any mask circuit pattern is not to be formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, said supporting region having first alignment marks used at the time of exposure of a mask made from said mask-making member for forming said mask circuit patterns thereon, second alignment marks being used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the step of:

forming all of said first alignment marks and said second alignment marks on said mask-making member at one time, said first alignment marks being formed in such a manner that one or more of said first alignment marks are located in a portion around each of said plurality of pattern formation regions of said supporting region, and said second alignment marks being formed in such a manner as to be all located in a portion outside an area formed by said plurality of said pattern formation regions of said supporting region.

13. (Cancelled)

14. (Original) A method of producing a mask-making member according to claim 12, wherein shapes of said first alignment marks are different from those of said second alignment marks.

15. (Original) A method of producing a mask-making member according to claim 12, wherein said mask-making member is a transmission mask-making member.

16. (Original) A method of producing a mask-making member according to claim 12, wherein said mask-making member is a stencil mask-making member.

17. (Previously Presented) A method of producing a mask-making member, said member has a plurality of pattern formation regions in which mask circuit patterns are to be formed, and a supporting region in which any mask circuit pattern is not to be formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, said supporting region having first alignment marks used at the time of exposure of a mask made from said mask-making member for forming said mask circuit patterns thereon, second alignment marks being used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the step of:

forming all of said first alignment marks and said second alignment marks on said mask-making member at one time, said first alignment marks being formed in such a manner that one or more of said first alignment marks are located in a portion around each of said plurality of pattern formation regions of said supporting region, and said second alignment marks being formed in such a manner as to be all located in a portion outside an area formed by said plurality of said pattern formation regions of said supporting region,

said mask-making member is a transmission mask-making member and said first alignment marks and said second alignment marks being formed on an electron scatterer formed on a membrane.

18. (Previously Presented) A method of producing a mask-making member, said member has a plurality of pattern formation regions in which mask circuit patterns are to be formed, and a supporting region in which any mask circuit pattern is not to be formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, said supporting region having first alignment marks used at the time of exposure of a mask made from said mask-making member for forming said mask circuit patterns thereon, second alignment marks being used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the step of:

forming all of said first alignment marks and said second alignment marks on said mask-making member at one time, said first alignment marks being formed in such a manner that one or more of said first alignment marks are located in a portion around each of said plurality of pattern formation regions of said supporting region, and said second alignment marks being formed in such a manner as to be all located in a portion outside an area formed by said plurality of said pattern formation regions of said supporting region, said mask-making member is a transmission mask-making member and said first alignment marks and said second alignment marks being formed on an electron scatterer being formed on a membrane by selectively removing said electron scatterer.

19. (Previously Presented) A method of producing a mask-making member, said member has a plurality of pattern formation regions in which mask circuit patterns are to be formed, and a supporting region in which any mask circuit pattern is not to be formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, said supporting region having first alignment marks used at the time of exposure of a mask made from said mask-making member for forming said mask circuit patterns thereon, second alignment marks being used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the step of:

forming all of said first alignment marks and said second alignment marks on said mask-making member at one time, said first alignment marks being formed in such a manner that one or more of said first alignment marks are located in a portion around each of said plurality of pattern formation regions of said supporting region, and said second alignment marks being formed in such a manner as to be all located in a portion outside an area formed by said plurality of said pattern formation regions of said supporting region, said mask-making member is a stencil mask-making member and said first alignment marks and said second alignment marks being formed on a mask board.

20. (Previously Presented) A method of producing a mask-making member, said member has a plurality of pattern formation regions in which mask circuit patterns are to be formed, and a supporting region in which any mask circuit pattern is not to be formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, said supporting region having first alignment marks used at the time of exposure of a mask made from said mask-

making member for forming said mask circuit patterns thereon, second alignment marks being used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the step of:

forming all of said first alignment marks and said second alignment marks on said mask-making member at one time, said first alignment marks being formed in such a manner that one or more of said first alignment marks are located in a portion around each of said plurality of pattern formation regions of said supporting region, and said second alignment marks being formed in such a manner as to be all located in a portion outside an area formed by said plurality of said pattern formation regions of said supporting region, said mask-making member is a stencil mask-making member and said first alignment marks and said second alignment marks are formed on a mask board by selectively removing said mask board.

21. (Previously Presented) A method of producing a mask-making member, said member has a plurality of pattern formation regions in which mask circuit patterns are to be formed, and a supporting region in which any mask circuit pattern is not to be formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, said supporting region having first alignment marks used at the time of exposure of a mask made from said mask-making member for forming said mask circuit patterns thereon, second alignment marks being used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the step of:

forming all of said first alignment marks and said second alignment marks on said mask-making member at one time, said first alignment marks being formed in such a

manner that one or more of said first alignment marks are located in a portion around each of said plurality of pattern formation regions of said supporting region, and said second alignment marks being formed in such a manner as to be all located in a portion outside an area formed by said plurality of said pattern formation regions of said supporting region, said mask-making member is a stencil mask-making member, and said first alignment marks and said second alignment marks being formed on a mask board by selectively removing said mask board to form holes or grooves in said mask board, and burying said holes or grooves with a metal whose atoms have atomic weights heavier than those of atoms of said mask board.

22. (Previously Presented) A method of producing a mask-making member, said member has a plurality of pattern formation regions in which mask circuit patterns are to be formed, and a supporting region in which any mask circuit pattern is not to be formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, said supporting region having first alignment marks used at the time of exposure of a mask made from said mask-making member for forming said mask circuit patterns thereon, second alignment marks being used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the step of:

forming all of said first alignment marks and said second alignment marks on said mask-making member at one time, said first alignment marks being formed in such a manner that one or more of said first alignment marks are located in a portion around each of said plurality of pattern formation regions of said supporting region, and said second alignment marks being formed in such a manner as to be all located in a portion outside an

area formed by said plurality of said pattern formation regions of said supporting region, said mask-making member is a stencil mask-making member and said first alignment marks and said second alignment marks being formed on a mask board by selectively removing said mask board to form holes or grooves in said mask board, and burying said holes or grooves with a metal whose atoms have atomic weights heavier than those of atoms of said mask board, and said metal is platinum, gold, silver, copper, tungsten, tantalum, or molybdenum.

23. (Previously Presented) A method of producing a mask-making member, said member has a plurality of pattern formation regions in which mask circuit patterns are to be formed, and a supporting region in which any mask circuit pattern is not to be formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, said supporting region having first alignment marks used at the time of exposure of a mask made from said mask-making member for forming said mask circuit patterns thereon, second alignment marks being used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the step of:

forming all of said first alignment marks and said second alignment marks on said mask-making member at one time, said first alignment marks being formed in such a manner that one or more of said first alignment marks are located in a portion around each of said plurality of pattern formation regions of said supporting region, and said second alignment marks being formed in such a manner as to be all located in a portion outside an area formed by said plurality of said pattern formation regions of said supporting region, and

the exposure of said mask-making member for forming said first alignment marks and said second alignment marks thereon at one time is performed by using a stepper type exposure system with a projected magnification of a 1:1 ratio or a low reduction ratio.

24. (Previously Presented) A method of producing a mask-making member, said member has a plurality of pattern formation regions in which mask circuit patterns are to be formed, and a supporting region in which any mask circuit pattern is not to be formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, said supporting region having first alignment marks used at the time of exposure of a mask made from said mask-making member for forming said mask circuit patterns thereon, second alignment marks being used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the step of:

forming all of said first alignment marks and said second alignment marks on said mask-making member at one time, said first alignment marks being formed in such a manner that one or more of said first alignment marks are located in a portion around each of said plurality of pattern formation regions of said supporting region, and said second alignment marks being formed in such a manner as to be all located in a portion outside an area formed by said plurality of said pattern formation regions of said supporting region, and the exposure of said mask-making member for forming said first alignment marks and said second alignment marks thereon at one time is performed by using a scanner type exposure system with a projected magnification of a 1:1 ratio or a low reduction ratio.

25. (Previously Presented) A method of producing a mask-making member, said member has a plurality of pattern formation regions in which mask circuit patterns are to be formed, and a supporting region in which any mask circuit pattern is not to be formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, said supporting region having first alignment marks used at the time of exposure of a mask made from said mask-making member for forming said mask circuit patterns thereon, second alignment marks being used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the step of:

forming all of said first alignment marks and said second alignment marks on said mask-making member at one time, said first alignment marks being formed in such a manner that one or more of said first alignment marks are located in a portion around each of said plurality of pattern formation regions of said supporting region, and said second alignment marks being formed in such a manner as to be all located in a portion outside an area formed by said plurality of said pattern formation regions of said supporting region, and the exposure of said mask-making member for forming said first alignment marks and said second alignment marks thereon at one time is performed by using a contact type full exposure system.

26. (Previously Presented) A method of producing a mask-making member, said member has a plurality of pattern formation regions in which mask circuit patterns are to be formed, and a supporting region in which any mask circuit pattern is not to be formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, said supporting region

having first alignment marks used at the time of exposure of a mask made from said mask-making member for forming said mask circuit patterns thereon, second alignment marks being used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the step of:

forming all of said first alignment marks and said second alignment marks on said mask-making member at one time, said first alignment marks being formed in such a manner that one or more of said first alignment marks are located in a portion around each of said plurality of pattern formation regions of said supporting region, and said second alignment marks being formed in such a manner as to be all located in a portion outside an area formed by said plurality of said pattern formation regions of said supporting region, and the exposure of said mask-making member for forming said first alignment marks and said second alignment marks thereon at one time is performed by using a proximity type full exposure system.

27. (Previously Presented) A method of producing a mask-making member, said member has a plurality of pattern formation regions in which mask circuit patterns are to be formed, and a supporting region in which any mask circuit pattern is not to be formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, said supporting region having first alignment marks used at the time of exposure of a mask made from said mask-making member for forming said mask circuit patterns thereon, second alignment marks being used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the step of:

forming all of said first alignment marks and said second alignment marks on said mask-making member at one time, said first alignment marks being formed in such a manner that one or more of said first alignment marks are located in a portion around each of said plurality of pattern formation regions of said supporting region, and said second alignment marks being formed in such a manner as to be all located in a portion outside an area formed by said plurality of said pattern formation regions of said supporting region, and the exposure of said mask-making member for forming said first alignment marks and said second alignment marks thereon at one time is performed by using a mirror-projections type full exposure system.

28. (Previously Presented) A method of producing a mask-making member, which member has a plurality of pattern formation regions in which mask circuit patterns are to be formed, and a supporting region in which any mask circuit pattern is not to be formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, said supporting region having first alignment marks used at the time of exposure of a mask made from said mask-making member for forming said mask circuit patterns thereon, second alignment marks being used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the steps of:

dividing all of said first alignment marks and said second alignment marks to be formed on said mask-making member into a plurality of groups each containing pluralities of said first alignment marks and said second alignment marks, and sequentially forming said alignment marks and said second alignment marks on said mask-making member by sequential exposure performed for each of said pluralities of groups.

29. (Original) A method of producing a mask-making member according to claim 28, wherein said first alignment marks are formed in such a manner that one or more of said first alignment marks are located in a portion, around each of said plurality of pattern formation regions, of said supporting region, and said second alignment marks are formed in such a manner as to be all located in a portion outside an area formed by said plurality of said pattern formation regions of said supporting region.

30. (Original) A method of producing a mask-making member according to claim 28, wherein shapes of said first alignment marks are different from those of said second alignment marks.

31. (Original) A method of producing a mask-making member according to claim 28, wherein said mask-making member is a transmission mask-making member.

32. (Original) A method of producing a mask-making member according to claim 28, wherein said mask-making member is a stencil mask-making member.

33. (Original) A method of producing a mask-making member according to claim 31, wherein said first alignment marks and said second alignment marks are formed on an electron scatterer formed on a membrane.

34. (Original) A method of producing a mask-making member according to claim 31, wherein said first alignment marks and said second alignment marks are formed on an electron scatterer formed on a membrane by selectively removing said electron scatterer.

35. (Original) A method of producing a mask-making member according to claim 32, wherein said first alignment marks and said second alignment marks are formed on a mask board.

36. (Original) A method of producing a mask-making member according to claim 32, wherein said first alignment marks and said second alignment marks are formed on a mask board by selectively removing said mask board.

37. (Original) A method of producing a mask-making member according to claim 32, wherein said first alignment marks and said second alignment marks are formed on a mask board by selectively removing said mask board to form holes or grooves in said mask board, and burying said holes or grooves with a metal whose atoms have atomic weights heavier than those of atoms of said mask board.

Claims 38-50 (Cancelled)

51. (Previously Presented) A method of making a mask according to claim 54, wherein said plurality of pattern formation regions are exposed to charged particle beams by using said first alignment marks for forming said mask circuit patterns on said plurality of pattern formation regions.

52. (Previously Presented) A method of making a mask, which mask has a plurality of pattern formation regions in which mask circuit patterns are formed, and a supporting region in which any mask circuit pattern is not formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, wherein said supporting region has first alignment marks used at the time of exposure of said mask for forming said mask circuit patterns thereon, second alignment marks used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the step of:

forming all of said first alignment marks and said second alignment marks on said mask at one time;

wherein said plurality of pattern formation regions are exposed to charged particle beams by using said first alignment marks for forming said mask circuit patterns on said plurality of pattern formation regions; and

wherein said exposure of said plurality of pattern formation regions to the charged particle beams is performed by using a charged particle beam exposure system configured such that the charged particle beam has a size of 10 μm or less and a maximum deflection width of the charged particle beam in a state that a stage on which an electron-optical system is mounted is not moved is larger than a total of a width of each of said plurality of pattern formation regions and a width of a portion between two of said plurality of pattern formation regions of said supporting region.

53. (Previously Presented) A method of making a mask according to claim 54, wherein said first alignment marks and said second alignment marks are covered with a protective film before exposure by the charged particle beams.

54. (Previously Presented) A method of making a mask, which mask has a plurality of pattern formation regions in which mask circuit patterns are formed, and a supporting region in which any mask circuit pattern is not formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, wherein said supporting region has first alignment marks used at the time of exposure of said mask for forming said mask circuit patterns thereon, second alignment marks used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the step of:

forming all of said first alignment marks and said second alignment marks on said mask at one time;

wherein said first alignment marks are formed in such a manner that one or more of said first alignment marks are located in a portion, around each of said plurality of pattern formation regions, of said supporting region, and said second alignment marks are formed in such a manner as to be all located in a portion outside an area formed by said plurality of said pattern formation regions of said supporting region.

55. (Previously Presented) A method of making a mask according to claim 54, wherein shapes of said first alignment marks are different from those of said second alignment marks.

56. (Previously Presented) A method of making a mask according to claim 54, wherein said mask is a transmission mask.

57. (Previously Presented) A method of making a mask according to claim 54, wherein said mask is a stencil mask.

Claims 58-60 (Cancelled)

61. (Currently Amended) A method of making a mask, which mask has a plurality of pattern formation regions in which mask circuit patterns are formed, and a supporting region in which any mask circuit pattern is not formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, wherein said supporting region has first alignment marks used at the time of exposure of said mask for forming said mask circuit patterns thereon, second alignment marks used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the step of:

forming all of said first alignment marks and said second alignment marks on said mask at one time;

~~wherein said mask is a stencil mask; and~~

wherein said first alignment marks and said second alignment marks are formed on a mask board by selectively removing said mask board to form holes or grooves in said mask board and burying said holes or grooves with a metal whose atoms have atomic weights heavier than those of atoms of said mask board.

62. (Previously Presented) A method of making a mask, which mask has a plurality of pattern formation regions in which mask circuit patterns are formed, and a supporting region in which any mask circuit pattern is not formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, wherein said supporting region has first alignment marks used at the time of exposure of said mask for forming said mask circuit patterns thereon, second alignment marks used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the step of:

forming all of said first alignment marks and said second alignment marks on said mask at one time;

wherein said mask is a stencil mask; and

wherein said first alignment marks and said second alignment marks are formed on a mask board by selectively removing said mask board to form holes or grooves in said mask board and burying said holes or grooves with a metal whose atoms have atomic weights heavier than those of atoms of said mask board.

63. (Original) A method of making a mask according to claim 62, wherein said metal is platinum, gold, silver, copper, tungsten, tantalum, or molybdenum.

64. (Previously Presented) A method of making a mask, which mask has a plurality of pattern formation regions in which mask circuit patterns are formed, and a supporting region in which any mask circuit pattern is not formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, wherein said supporting region has first alignment

marks used at the time of exposure of said mask for forming said mask circuit patterns thereon, second alignment marks used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the step of:

forming all of said first alignment marks and said second alignment marks on said mask at one time;

wherein the exposure of said mask for forming said first alignment marks and said second alignment marks thereon at one time is performed by using a stepper type exposure system with a projected magnification of a 1:1 ratio or low reduction ratio.

65. (Previously Presented) A method of making a mask, which mask has a plurality of pattern formation regions in which mask circuit patterns are formed, and a supporting region in which any mask circuit pattern is not formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, wherein said supporting region has first alignment marks used at the time of exposure of said mask for forming said mask circuit patterns thereon, second alignment marks used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the step of:

forming all of said first alignment marks and said second alignment marks on said mask at one time;

wherein the exposure of said mask for forming said first alignment marks and said second alignment marks thereon at one time is performed by using a scanner type exposure system with a projected magnification of a 1:1 ratio or a low reduction ratio.

66. (Previously Presented) A method of making a mask, which mask has a plurality of pattern formation regions in which mask circuit patterns are formed, and a supporting region in which any mask circuit pattern is not formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, wherein said supporting region has first alignment marks used at the time of exposure of said mask for forming said mask circuit patterns thereon, second alignment marks used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the step of:

forming all of said first alignment marks and said second alignment marks on said mask at one time;

wherein the exposure of said mask for forming said first alignment marks and said second alignment marks thereon at one time is performed by using a contact type full exposure system.

67. (Cancelled)

68. (Previously Presented) A method of making a mask, which mask has a plurality of pattern formation regions in which mask circuit patterns are formed, and a supporting region in which any mask circuit pattern is not formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, wherein said supporting region has first alignment marks used at the time of exposure of said mask for forming said mask circuit patterns thereon, second alignment marks used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the step of:

forming all of said first alignment marks and said second alignment marks on said mask at one time;

wherein the exposure of said mask for forming said first alignment marks and said second alignment marks thereon at one time is performed by using a mirror-projection type full exposure system.

69. (Previously Presented) A method of making a mask, which mask has a plurality of pattern formation regions in which mask circuit patterns are formed, and a supporting region in which any mask circuit pattern is not formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, said supporting region having first alignment marks used at the time of exposure of said mask for forming said mask circuit patterns thereon, second alignment marks being used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said method comprising the step of:

dividing all of said first alignment marks and said second alignment marks to be formed on said mask into a plurality of groups each containing pluralities of said first alignment marks and said second alignment marks and sequentially forming said first alignment marks and said second alignment marks on said mask by sequential exposure performed for each of said pluralities of groups.

70. (Original) A method of making a mask according to claim 69, wherein each relative distance between two of said plurality of groups is obtained by measuring each relative distance between said first alignment marks located in the two of said plurality of groups and each relative distance between said second alignment marks located in the two of

said plurality of groups and the exposure by the charged particle beams for forming said mask circuit patterns on said plurality of regions is performed by using said first alignment marks corrected on the basis of the measured results.

71. (Original) A method of making a mask according to claim 70, wherein said first alignment marks and said second alignment marks are covered with a protective film before exposure by the charged particle beams.

72. (Original) A method of making a mask according to claim 69, wherein said first alignment marks are formed in such a manner that one or more of said first alignment marks are located in a portion, around each of said plurality of pattern formation regions, of said supporting region and said second alignment marks are formed in such a manner as to be all located in a portion, outside an area formed by said plurality of said pattern formation regions, of said supporting region.

73. (Original) A method of making a mask according to claim 69, wherein shapes of said first alignment marks are different from those of said second alignment marks.

74. (Original) A method of making a mask according to claim 69, wherein said mask is a transmission mask.

75. (Original) A method of making a mask according to claim 69, wherein said mask is a stencil mask.

76. (Original) A method of making a mask according to claim 74, wherein said first alignment marks and said second alignment marks are formed on an electron scatterer formed on a membrane.

77. (Original) A method of making a mask according to claim 74, wherein said first alignment marks and said second alignment marks are formed on an electron scatterer formed on a membrane by selectively removing said electron scatterer.

78. (Original) A method of making a mask according to claim 75, wherein said first alignment marks and said second alignment marks are formed on a mask board.

79. (Original) A method of making a mask according to claim 75, wherein said first alignment marks and said second alignment marks are formed on a mask board by selectively removing said mask board.

80. (Original) A method of making a mask according to claim 75, wherein said first alignment marks and said second alignment marks are formed on a mask board by selectively removing said mask board to form holes or grooves in said mask board, and burying said holes or grooves with a metal whose atoms have atomic weights heavier than those of atoms of said mask board.

81. (Original) A method of making a mask according to claim 80, wherein said metal is platinum, gold, silver, copper, tungsten, tantalum or molybdenum.

82. (Previously Presented) A method of making a mask, which mask has a plurality of pattern formation regions in which mask circuit patterns are formed, and a supporting region in which any mask circuit pattern is not formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, said supporting region having first alignment marks used at the time of exposure of said mask for forming said mask circuit patterns thereon, second alignment marks being used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said second alignment marks being used for exposure of a substrate to be exposed by a charged particle beam reduction-and-division transfer exposure system by using said second alignment marks, said method comprising the steps of:

performing exposure of a substrate to be exposed by said charged particle beam reduction-and-division transfer exposure system by using a test mask having a positional deviation measurement pattern, to dividedly transfer said positional deviation measurement pattern on said substrate at a specific reduction ratio;

obtaining a positional deviation amount of said charged particle beam reduction-and-division transfer exposure system upon exposure and a correction amount for correcting the positional deviation amount by using the positional deviation measurement pattern which has been dividedly transferred on said substrate at the specific reduction ratio; and

performing exposure of said mask for forming said mask circuit patterns while correcting said mask circuit patterns by the correction amount for the positional deviation so as to correct the positional deviation amount of said charged particle beam reduction-and-division transfer exposure system, to thereby correct said mask.

83. (Cancelled)

84. (Previously Presented) An exposure process comprising the steps of:

producing a mask having a plurality of pattern formation regions in which mask circuit patterns are formed, and a supporting region in which any mask circuit pattern is not formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, said supporting region having first alignment marks used at the time of exposure of said mask for forming said mask circuit patterns thereon, second alignment marks being used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon; and performing exposure of a substrate to be exposed by a charged particle beam reduction-and-division transfer exposure system using said second alignment marks formed on said mask

wherein,

a substrate to be exposed is exposed by said charged particle beam reduction-and-division transfer exposure system by using a test mask having a positional deviation measurement pattern, to dividedly transfer said positional deviation measurement pattern on said substrate at a specific reduction ratio;

a positional deviation amount of said charged particle beam reduction-and-division transfer exposure system upon exposure and a correction amount for correcting the positional deviation amount are obtained by using the positional deviation measurement pattern which has been dividedly transferred on said substrate at the specific reduction ratio;

exposure of said mask for forming said mask circuit patterns thereon while correcting said mask circuit patterns by the correction amount for the positional deviation is

performed so as to correct the positional deviation amount of said charged particle beam reduction-and-deviation transfer exposure system, to thereby correct said mask; and

exposure of a substrate to be exposed by said charged particle beam reduction-and-division transfer exposure system is performed by using said corrected mask.

85. (Original) An exposure process according to claim 84, wherein a substrate to be exposed is exposed by each of a plurality of charged particle beam reduction-and-division transfer exposure systems by using the same test mask having a positional deviation measurement pattern, to dividedly transfer said positional deviation measurement pattern on said substrate at a specific reduction ratio;

a positional deviation amount of each of said plurality of charged particle beam reduction-and-deviation transfer exposure systems upon exposure and a correction amount for correcting the positional deviation amount are obtained by using the positional deviation measurement pattern which has been dividedly transferred on said substrate at the specific reduction ratio;

exposure of said mask for forming said mask circuit patterns thereon while correcting said mask circuit patterns by the correction amount for the positional deviation is performed so as to correct the positional deviation of each of said plurality of charged particle beam reduction-and-division transfer exposure systems, to thereby correct said mask for each of said plurality of charged particle beam reduction-and-division transfer exposure systems; and,

exposure of a substrate to be exposed is performed by said plurality of charged particle beam reduction-and-division transfer exposure systems using said corrected masks.

86. (Previously Presented) A method of fabricating a semiconductor device comprising:

a plurality of exposure steps in each of which exposure of a semi-conductor substrate is performed by a charged particle beam reduction-and-division transfer exposure system using a plurality of masks, each of said masks having a plurality of pattern formation regions in which mask circuit patterns are formed, and a supporting region in which any mask circuit pattern is not formed, said supporting region being provided for holding said plurality of pattern formation regions while separating said plurality of pattern formation regions from each other, wherein said supporting region has first alignment marks used at the time of exposure of said mask for forming said mask circuit patterns thereon, ~~and~~ second alignment marks used at the time of exposure of a substrate to be exposed for forming circuit patterns thereon, said first alignment marks and said second alignment marks are formed on each of said plurality of masks used for said plurality of exposure steps by using the same master mask.